IN THE SPECIFICATION

Page 3, please replace the paragraph at lines 3-16 as follows:

As shown in FIG. 1A, an n+-type buffer layer 11, an n -type base layer 12, and a p-type base layer 13 are formed in the order mentioned on a p+-type collector layer 10. Also, an n+-type emitter layer 14 is in a part of the surface region of the p-type base layer 13. Also formed is a trench 15 extending downward from the surface of the emitter layer 14 to reach the n -type base layer 12 through the emitter layer 14 and the p-type base layer 13. A gate electrode 17 (trench-gate electrode), which is covered with a gate insulating film 16, is buried in the trench 15. The trench-gate electrode 17 is withdrawn to reach, for example, a pad (not shown) for the gate electrode for contact with the outside.

Page 3, please replace the paragraph at lines 17-26 as follows:

An emitter electrode 18 is formed to cover the emitter layer 14 and the p-type base layer 13. The emitter layer 14 and the p-type base layer 13 are electrically short-circuited by the emitter electrode 18. Also, an insulating film 19 is formed on the trench-gate electrode 17. The trench-gate electrode 17 and the emitter electrode 18, are electrically isolated from each other by the insulating film 19. Also, a collector electrode 20 is formed on the back surface of the collector region 10.

Delete page 12, line 18 to page 15, line 13.

Amend page 15, lines 14-16 to read:

A semiconductor element according to an aspect of the invention comprises:

Delete page 15, line 14 to page 16, line 19.

Amend page 16, lines 20-22 to read:

A method of fabricating a semiconductor element according to an aspect of the present invention comprises:

Delete page 17, line 20 to page 22, line 9.

Page 22, please delete the paragraph at lines 11-17.

Page 28, please replace the paragraph at line 18 to page 29, line 17 as follows:

As shown in the drawing, an n+-type buffer layer 41, an n -type base layer 42 having a high resistivity, a p+-type base layer 51 having a high impurity concentration, and a p-type base layer 43 having a low impurity concentration are formed in the order mentioned on one surface region of a p+-type collector layer 40. Also, an n+-type emitter layer 44 is selectively formed in a part of the surface region of the p-type base layer 43. Further, a trench 45 is formed to extend downward from the surface of the emitter layer 14 to reach the n -type base layer 42 through the emitter layer 44, the p-type base layer 43 and the p+-type base layer 51. A gate electrode 47 (trench-gate electrode), which is covered with a gate insulating film 46, is buried in the trench 45. Incidentally, the emitter layer 44 is formed to have, for example, a striped pattern consisting of a plurality of columns as viewed from above, and the trench 45 is formed in a middle region of adjacent the emitter layers 44. In other words, each of the trench 45 and the trench-gate electrode 47 is also formed to have a striped pattern consisting of a plurality of columns as viewed from above. Also, the p+-type collector layer 40 consists of a p+-type silicon substrate, and each of the n+-type buffer layer 41 and the n -type base layer 42 consists of an epitaxially grown layer formed on the p+-type silicon substrate.

Page 34, please replace the paragraph at lines 10-21 as follows:

In the IGBT according to this embodiment, the threshold voltage is determined by the p+-type base layer 51 having the impurity concentration higher than that of the p-type base layer 43 and, thus, the pinch off phenomenon also takes place in the p+-type base layer 51 having a high impurity concentration. It should be noted that the p+-type base layer 51 is formed in a location deeper than the junction between the emitter layer 44 and the p-type base layer 43. In other words, the pinch-off point is located closer to the n-type base layer in the embodiment of the present invention than in the prior art.

Page 34, please replace the paragraph at line 23 to page 35, line 13 as follows:

As described above, the pinch-off point is controlled by forming the p+-type base layer 51. The significance of the particular control will now be described in detail with reference to the graph of FIG. 3C. In the graph of FIG. 3C, the position in the depth direction, as measured from the boundary between the emitter electrode and the emitter layer, is plotted in the abscissa. Also, the voltage, as measured on the basis of the voltage at the boundary between the emitter electrode and the emitter layer, is plotted on the ordinate of the graph. The voltage distribution over the various regions is plotted in the graph of FIG. 3C in respect of the conventional IGBT and the IGBT according to this embodiment of the present invention. Incidentally, the point in the depth direction is plotted simply as a model on the abscissa of the graph. In general, the emitter layer is actually formed very thin, compared with, for example, the p-type base layer.

Page 36, please replace the paragraph at lines 10-27 as follows:

As described above, it is possible to decrease the collector voltage VCE by setting the pinch-off point in a deep position inside the p-type base layer so as to diminish the saturation value of the collector current because the saturation value of the collector current of the IGBT is basically changed in proportion to the square of the collector voltage VCE. FIG. 3D shows the result of simulation of the static characteristics in terms of the relationship between the collector voltage and the collector current in respect of the conventional IGBT and the IGBT according this embodiment of the present invention. As shown in FIG. 3D, the saturation current value of the IGBT according to this embodiment is lower than that of the conventional IGBT. It follows that it is possible in the embodiment of the present invention to suppress the amount of heat generated by the saturation current, making it possible to improve the short circuit withstand capability.

Page 43, please replace the paragraph at line 21 to page 44, line 12 as follows:

The ion implantation method and annealing, which is widely used for forming an impurity diffusion layer, can also be used in the embodiment of the present invention for forming the p-type base layer. It is known to the art that, if the accelerating voltage of the impurity in the ion implantation step is increased, the concentration peak of the impurity is changed. Therefore, where the high concentration p+-type base 51 layer is formed by the ion implantation and annealing, it is necessary to set the accelerating voltage such that it is possible to obtain a desired short circuit withstand capability. Table 2 shows the result of simulation of the relationship between the accelerating voltage and the short circuit withstand capability.

Page 47, please replace the paragraph at lines 3-9 as follows:

It should be noted, however, that it is not absolutely necessary for gl and g2 to satisfy the relationship of g2 > gl. As far as it is possible to move the pinch-off point closer to the n^--type base layer than in the prior art, it is possible to diminish the value of V(pin-ch) in VCE so as to obtain the effect the embodiment of the present invention.

Page 71, please replace the paragraph at lines 18-25 as follows:

According to the power MOSFET according to this embodiment of the present invention, however, it is possible to diminish the saturation current value in the event of the load short circuit, with the result that it is possible to increase the short circuit withstand capability. The reason for the improvement in the short circuit withstand capability achieved in the embodiment of the present invention will now be described.

Page 74, please replace the paragraph at line 26 to page 75, line 11 as follows:

In other words, the channel conductance g3 between the pinch-off point Q of the p+-type base layer 80 and the n+-type source layer 73 is not larger than the channel conductance g4 between the pinch-off point Q and the n -type base layer 71. In short, the relationship of g4 > g3 is established in the power MOSFET of the embodiment of the present invention in

contrast to the relationship of g4 < g3 for the prior art. As a result, it is possible to diminish the drain voltage VDS, at which the pinch-off phenomenon is generated, compared with the prior art, so as to diminish the saturation current value and, thus, to improve the short circuit withstand capability of the power MOSFET.

Page 75, please replace the paragraph at lines 12-19 as follows:

Incidentally, the technical idea of the embodiment of the present invention can also be applied to the case where the n-type drain layer 70 and the drain electrode 79 are formed flush with the n-type source layer 73 and the source electrode 77. Further, it is possible to apply the trench contact structure described previously in conjunction with the examples of IGBT to the MOSFET according to this embodiment of the present invention.

Page 75, please replace the paragraph at lines 20-26 as follows:

As described above in conjunction with the first to tenth embodiments of the present invention, the embodiment of the present invention makes it possible to improve the short circuit withstand capability of the power semiconductor elements such as IGBT and the power MOSFET without inviting deterioration of the on-voltage characteristics.

Page 75, please replace the paragraph beginning at line 27 to page 76, line 13 as follows:

The technical idea of the embodiment of the present invention resides in that the pinch-off phenomenon is generated in a position closer to the n-type base layer than in the prior art. It should be noted that it is not absolutely necessary to meet the condition of Cpl > Cp2 in the impurity concentration profile shown in, for example, FIG. 4F. Cpl can be equal to Cp2, i.e., Cpl = Cp2, or can be smaller than Cp2, i.e., Cpl < Cp2. This is because the MOSFET has a threshold voltage that is lower at a position near the n-type base layer than at the junction between the emitter layer and p-type base layer. (hereinafter, this junction will be referred to as "point J111, shown in FIG. 3A and FIG. 3B.)

Page 97, please replace the paragraph at lines 15-19 as follows:

As described above, the saturation current value can be decreased in the embodiment of the present invention by controlling the pinch-off point in the channel region, making it possible to improve the short circuit withstand capability of the power semiconductor element.